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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/817,842	03/26/2001	Robert F. Gazdzinski	RFG.006CP1	9452

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GAZDZINSKI & ASSOCIATES
11440 WEST BERNARDO COURT, SUITE 375
SAN DIEGO, CA 92127

EXAMINER	
LEUBECKER, JOHN P	

ART UNIT	PAPER NUMBER
3739	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/817,842	GAZDZINSKI, ROBERT F.	
	Examiner	Art Unit	
	John P. Leubecker	3739	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-26,34-41 and 46-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-26,34-41 and 46-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/16/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 16, 36, 39 and 53 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 16, although the description of "optimization" (i.e., selecting a processor core ...) appears to be a process step and is given little or no patentable weight with respect to the claimed structure (as discussed below), the term "extension" is vague and indefinite (perhaps "extension instruction" was intended since this is supported by the specification).

As to claim 36, the phrase "having a spreading code that is substantially unique from any other spreading code" is indefinite as to the intended meaning. This would appear to be self-fulfilling (i.e., any particular code is unique from any other one, since they are not the same; unless they are the same, and then they wouldn't be unique).

As to claim 39, term "extensions" is vague and indefinite, thus making what is meant by a hardware extension (this term is not in the specification) or a software extension (not in spec. but "extension instruction" is) not readily known.

As to claim 53, comparison of the processor cycles to "that required by a general purpose instruction useful for the same purpose" is indefinite since there is no readily recognizable reference or standard for "general purpose instruction useful for the same purpose", making the scope of the claim unclear.

Note

3. It is noted that claims 16, 39, 40, 52 and 53 are product by process claims (or is a product claim which includes a process step). In such claims process limitations are given little or no patentable weight. The method of forming the product is not germane to the issue of patentability of the product itself. Further, when the prior art discloses a product which reasonably appears to be either identical with or only slightly different than a product claim in a product-by-process claim, the burden is on the Applicant to present evidence from which the Examiner could reasonably conclude that the claimed product differs in kind from those of the prior art. *In re Brown*, 459 F.2d 531, 173 USPQ 685 (CCPA 1972); *In re Fessman*, 489 F.2d 742, 180 USPQ 324 (CCPA 1974). This burden is NOT discharged solely because the product was derived from a process not known to the prior art. *In re Fessman*, 489 F.2d 742, 180 USPQ 324 (CCPA 1974).

Claim Rejections - 35 USC § 102

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 35, 38-41, 46, 48 and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by Brune (U.S. Pat. 5,984,875) for the reasons set forth in numbered paragraph 7 of the previous Office Action, paper number 01062006.

Although the Examiner could find no evidence of a maximum size for a semi-conductive die (as noticed by Applicant, the Examiner erroneously left off the word "semi" in the previous

Office Action), and still takes the position that the a circuit board of Brune, which is in part, semi-conductive by nature, and is die-like (flat, wafer shaped) in shape, meets the limitations of a single semi-conductive die, it is noted that each chip (i.e., microprocessor U1, oscillator U4, etc.) comprises at least on die. As to claim 38, although not given any patentable weight, the design of the data processor, and any other circuitry for that matter, had to consider size and power consumption by nature of it being "designed". As to claim 39, the device of Brune is designed to be "inductively programmed" which inherently includes hardware for the downloading of software (although it is not clear what a hardware extension is, it is assumed that a software extension is an instruction, as per the specification) (note col.6, lines 25-30).

6. Claims 15, 16, 30, 35, 38-41, 46 and 50-53 are rejected under 35 U.S.C. 102(b) as being anticipated by Alfano et al. (U.S. Pat. 6,240,312) for the reasons set forth in numbered paragraph 8 of the previous Office Action, paper number 01062006.

Regarding the newly added limitations, note col.5, line 66 to col.6, line 12 which suggests placing a data processor and communications device on the "same die".

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 15-20, 23, 35, 40, 41 and 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Banyai et al. (U.S. Pat. 6,128,220).

Brune discloses the device as described in numbered paragraph 7 of the previous Office Action, paper number 01062006. Notwithstanding the fact that the components of Brune are all formed on a single circuit board (note above) and thus, as applicable to claim 40, are designed to be "adapted to be integrated", the components of Brune are not incorporated in one integrated chip which includes a single die. However, the integration of components is "well within the capability of those skilled in the semiconductor design and fabrication arts", as admitted by Applicant (note specification, page 31, lines 3-14). Banyai et al. teaches that by integrating separate components (e.g., memory) on the same die as a microprocessor, the design "reduces cost and complexity because of the elimination of hardware required and the additional serial protocol required to communicate with an off-chip memory device". The Examiner takes the position that this concept of integration would, to anyone of ordinary skill, apply to any combinable set of discrete components, including the discrete circuitry of the communications device in Brune. It would have therefore been obvious to one of ordinary skill in the art to have provided the discrete components of Brune on a single semi-conductive die (IC chip die) for the reasons taught by Banyai et al.

9. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Banyai et al., as set forth above, and further in view of Kratz et al. (U.S. Pat. 4,061,461) for the reasons set forth in numbered paragraph 10 of the previous Office Action, paper number 01062006.

10. Claims 24, 25 and 34 rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Banyai et al., as set forth above, and further in view of Souissi et al. (U.S. Pat. 5,671,247) for the reasons set forth in numbered paragraph 11 of the previous Office Action, paper number 01062006.

11. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Banyai et al., as set forth above, and further in view of Roberts et al. (U.S. Pat. 6,636,566) or the PulsON article (note item 60 in Applicant's IDS) for the reasons set forth in numbered paragraph 12 of the previous Office Action, paper number 01062006.

12. Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Souissi et al. for the reasons set forth in numbered paragraph 11 of the previous Office Action, paper number 01062006.

13. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Kratz et al. for the reasons set forth in numbered paragraph 10 of the previous Office Action, paper number 01062006.

14. Claims 49 and 55 rejected under 35 U.S.C. 103(a) as being unpatentable over Alfano et al. in view of Seiko Epson Corp. (JP 2-82889) for the reasons set forth in numbered paragraph 14 of the previous Office Action, paper number 01062006.

15. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brune in view of Banyai et al., as set forth above, and further in view of Fette et al. (U.S. Pat. 4,862,407) for the reasons set forth in numbered paragraph 13 of the previous Office Action, paper number 01062006.

16. Other analogous rejections under 35 USC 103(a) over Alfano et al. in view of certain references used in relation to the Brune reference could be made on certain claims concerning the application of known technology. However, since these claims have been rejected and the Examiner is only given an limited amount of time, no matter how overly broad the claims, they will not be made until necessary, or until what is considered the invention is made clear to the Examiner.

Response to Arguments

17. Applicant's arguments filed June 16, 2006 have been fully considered but they are not persuasive.

Regarding claim 15 over Brune, and as mentioned above, leaving the word "semi" off of "semiconductive" actually was not any convenience at all, just a typo. The Examiner's position regarding this term is set forth above. Even so, the Examiner respectfully disagrees with Applicant with respect to not being able to "claim inherent teaching".(page 7, line 23 of Applicant's remarks) since Brune discloses IC chips in the capsule design and, correct the Examiner if he is wrong, these IC chips would include a least one die. It is noted that the previous claim did not require that the data processor and communications device be *formed on a*

single semiconductive die as now claimed but just had to include one. In any event, the Examiner addresses the newly added limitation above.

As a side note, the Examiner wishes to point out that the term "die", especially as known in the integrated circuit arts, does not necessarily have to refer to a *single* piece of semiconductive material but could refer to multiple dies.

Furthermore, the Examiner respectfully disagrees that Brune's choice of components "teaches away" from use in a human being. The Examiner could not find any evidence that necessarily excluded the Brune device from such use. In any event, the Examiner is relying on the structural elements of Brune and not its intended use.

Regarding Applicant's suggestion that he discovered the "source of a problem" (e.g., reduction in physical size and power consumption), the Examiner was not aware of such problem since the integrated circuit and communications technology was known well before the time of the invention, as pointed out by the numerous references to known technology in Applicant's specification. Applicant did not provide evidence that miniaturization was a "problem" in the art.

Regarding claim 16, the Examiner maintains the position that any data processor inherently includes a core which has a certain power consumption which is "reduced" compared to what it could be and is thus optimized. Any design for size and power consumption is its own optimal design by nature of being the preferred or chosen design. No one in their right mind would design and inefficient, larger than it has to be, power wasting component.

Regarding claim 15 and the Alfano reference, Applicant does not appear to get the "gist" of the Examiner's rejections at all (note page 9, lines 12-16 of Applicant's arguments). Previous

claim 15 did not require the processor and communications device on "the same die" and the Examiner did not describe it this way. However, it just so happens that Alfano does describe such structure (note col.5, line 66 to col.6, lines 12).

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wishart et al. (U.S. Pat. 5,293,329)—note col.1, lines 30-34 ("The focus is always on reducing the computational complexity of the architecture, and hence the ASIC mass and power requirements. Many efficient architectures are based on the use of an FFT to simultaneously demultiplex or multiplex a block of signal channels")

Gauglitz (U.S. Pat. 5,231,990)—note col. 13, lines 15-55 regarding integration using ASICs.

DePauli (U.S. Pat. 4,963,793)—note col.4,lines 26-43 regarding optimizing a microprocessor using an ASIC ("The manufacture of an ASIC reduces cost through reduced complexity and may require less power to operate").

Dowling (U.S. Pat. 6,226,738)—note cpu with DRAM on single die.

Hopkinson et al. (U.S. Pat. 6,081,821)—note col.2, lines 10-16 ("The application-specific integrated circuits (ASICs) which implement the present invention allow flexible, high-precision, high-performance FFT processors to be realized. Unlike prior art commercial FFT offerings, the processor of the present invention incorporates all FFT support functions--including coefficient and memory-address generation--on a single die.")

Yuen (U.S. Pat. 5,367,187)—note col.1, line 56 to col. 2, line 2 ("an application specific integrated circuit (ASIC) manufacturer would typically have to store an inventory of gate array architectures of different sizes, each of which has a respective capacity sufficient to accommodate up to some maximum number of gate cells. Thus, to efficiently map a completed circuit design into an integrated circuit architecture, the circuit designer would select, from an inventory of pre-established gate array die sizes (e.g., 1K, 2.5K, 5K, 7.5K, 10K and 20K gate cell arrays), the die size is selected such that it includes at least the number of gates required for a completed circuit design.")

Fiocca (U.S. Pat. 5,625,743—note col.8, lines 8-24.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Leubecker whose telephone number is (571) 272-4769. The examiner can normally be reached on Monday through Friday, 6:00 AM to 2:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Linda C.M. Dvorak can be reached on (571) 272-4764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John P. Leubecker
Primary Examiner
Art Unit 3739

jpl